Please amend the application as follows:

In the Claims:

Please amend the claims as follows:

1. (three times amended) An integrated circuit package comprising:

a multilayer substrate comprising a top layer having a top surface and a bottom layer having a bottom surface opposite said top surface, said top and said bottom layers having a plurality of overlapping peripheral openings, wherein said openings are larger in said top layer than in said bottom layer such that a portion of a top surface of said bottom layer is exposed;

a plurality of routing strips on said top surface of said bottom layer, wherein at least one of said routing strips is on said exposed portion of said top surface of said bottom layer;

a chip adhered to said bottom surface of said bottom layer of said substrate;

a plurality of electrical conductors physically attached to said chip and located such that each electrical conductor in said plurality of electrical conductors is aligned within a respective one of said plurality of peripheral openings in said substrate;

a plurality of pads disposed on said top surface of said top layer of said substrate generally centralized within said peripheral openings of said substrate; and

potting material filling said peripheral openings.

2. (cancelled)

3. (amended) The integrated circuit package as recited in claim 1 wherein at least one of said pads disposed on said top surface of said top layer of said substrate is electrically connected with said at least one of said routing strips.

4. (amended) The integrated circuit package as recited in claim 3 wherein at least one of said pads disposed on said top surface of said top layer of said substrate is electrically connected with said at least one of said routing strips with a via through said top layer of said substrate.

8. (twice amended) An integrated circuit package comprising:

a multilayer substrate comprising a top layer having a top surface and a bottom layer having a bottom surface opposite said top surface, said top and said bottom layers having a plurality of overlapping peripheral openings, wherein said openings are larger in said top layer than in said bottom layer such that a portion of a top surface of said bottom layer is exposed;

a plurality of routing strips on said top surface of said bottom layer, wherein at least one of said routing strips is on said exposed portion of said top surface of said bottom layer;

a plurality of pads disposed centrally on said top surface, at least one of said pads being electrically connected with said at least one of said routing strips;

potting material filling said plurality of peripheral openings;

a chip having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate; and

wire bonding electrically connecting said chip to said substrate between at least one of said bonding pads and said at least one of said routing strips on said exposed portion of said top surface of said bottom layer.

15. (amended) The integrated circuit package as recited in claim 8 wherein said at least one of said pads being electrically connected with said at least one of said routing strips is connected by a via through said top layer of said substrate.

20. (amended) The integrated circuit package as recited in claim 19, wherein said peripheral openings in said second layer are larger than the peripheral openings in said first layer, such that a portion of a top surface of said first layer is exposed in each of said peripheral openings in said second layer.

22. (amended) An integrated circuit package comprising:

a substrate having a plurality of peripheral openings and first and second surfaces;

a chip comprising an operative side and a non-operative side, wherein said chip is adhered to said second surface of said substrate such that the non-operative side faces away from the substrate;

a plurality of pads disposed on said first surface of said substrate within said peripheral openings of said substrate, said substrate having a substantially similar size to that of said chip such that no pads of said plurality of pads may be located on said substrate between said peripheral openings and an outside edge of said substrate; and

potting material filling said peripheral openings.

REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 1-22 were pending in this application. Claim 2 has been cancelled. Claims 1, 3, 4, 8, 15, 20, and 22 have been amended to better define the scope of the claimed invention.

The drawings were objected to as not showing aspects of Claims 16 and 21 involving "first, second, and third layers." Applicant believes that the objection should have been addressed to Claims 15 and 20, which included those

features, rather than Claims 16 and 21. Claims 15 and 20 have been amended such that the objection is now moot.

Claims 1-10, 12, and 22 stand rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura, et al. (U.S. Patent No. 5,777,391). Claim 1 includes the features of "a multilayer substrate comprising a top layer having a top surface and a bottom layer having a bottom surface opposite said top surface, said top and said bottom layers having a plurality of overlapping peripheral openings, wherein said openings are larger in said top layer than in said bottom layer such that a portion of a top surface of said bottom layer is exposed." Nakamura does not teach or suggest such a multilayer substrate. In addition, Claim 1 includes the feature of "a plurality of routing strips on said top surface of said bottom layer, wherein at least one of said routing strips is on said exposed portion of said top surface of said bottom layer." Nakamura does not teach or suggest routing strips on a multilayer substrate exposed in this manner. Therefore, Applicant respectfully submits that Claim 1 is patentable over Nakamura. Claim 2 has been cancelled. Claim 3 depends from Claim 1 and is therefore patentable over Nakamura for at least the reasons presented above for that claim.

Claim 4 includes the feature "wherein at least one of said pads disposed on said first surface of said substrate is electrically connected with said at least one of said routing strips with a via through said top layer of said substrate." Nakamura does not teach or suggest the use of vias in such a manner. Claims 5-7 depend from Claim 1 and are therefore patentable over Nakamura for at least the reasons presented above for that claim.

Claim 8 includes the feature of "wire bonding electrically connecting said chip to said substrate between at least one of said bonding pads and said at least one of said routing strips on said exposed portion of said top surface of said bottom layer." Nakamura does not teach or suggest such a feature. Claims 9, 10, and 12 depend from Claim 8 and are therefore patentable over Nakamura for at least the reasons presented above for that claim.

Claim 22 includes the feature of "a plurality of pads disposed on said first surface of said substrate within said peripheral openings of said substrate, said substrate having a substantially similar size to that of said chip such that no pads of said plurality of pads may be located on said substrate between said peripheral openings and an outside edge of said substrate." Nakamura does not teach or suggest such a feature. Nakamura's substrate shown in Figures 1-4 is substantially larger than the chip and includes pads outside the openings between the openings and the edge of the substrate.

Claims 14-16 and 19-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Barrow (U.S. Patent No. 4,560,962). Claim 14 depends from Claim 8. As argued above, Nakamura fails to teach or suggest all of the features of Claim 8. Barrow does not cure this deficiency of Nakamura as Barrow was cited by the Examiner for its teachings of various substrate layers thicknesses. Since the proposed combination references fails to teach or suggest all of the claimed features, Applicant respectfully submits that Claim 14 is patentable over those references at least by virtue of its dependency on Claim 8. Claim 15 has been amended such that the rejection of that claim is now moot.

Claim 16 includes the feature of "said chip having an outline that is substantially the same as said outline of said substrate." Nakamura does not teach or suggest such a feature. Barrow, cited for its teachings of layers thicknesses, does not cure the deficiencies of Nakamura in this regard. Claim 16 also includes the feature of "vias connecting said routing strips to said pads." Nakamura does not teach or suggest such a feature. Barrow, cited for its teachings of layers thicknesses, does not cure the deficiencies of Nakamura in this regard. Therefore, Applicant respectfully submits that Claim 16 is patentable over the proposed combination of references.

Claim 19 depends from Claim 16. As argued above, Nakamura fails to teach or suggest all of the features of Claim 16. Barrow does not cure this deficiency of Nakamura as Barrow was cited by the Examiner for its teachings of

various substrate layers thicknesses. Since the proposed combination references fails to teach or suggest all of the claimed features, Applicant respectfully submits that Claim 19 is patentable over those references at least by virtue of its dependency on Claim 16. Claim 20 has been amended such that the rejection of that claim is now moot.

Claim 21 depends from Claim 1. As argued above, Nakamura fails to teach or suggest all of the features of Claim 1. Barrow does not cure this deficiency of Nakamura as Barrow was cited by the Examiner for its teachings of various substrate layers thicknesses. Since the proposed combination references fails to teach or suggest all of the claimed features, Applicant respectfully submits that Claim 21 is patentable over those references at least by virtue of its dependency on Claim 1.

Claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Imamura, et al. (U.S. Patent No. 5,512,786). Claim 11 depends from Claim 8. As argued above, Nakamura fails to teach or suggest all of the features of Claim 8. Imamura does not cure this deficiency of Nakamura as Imamura was cited by the Examiner for its teachings of various solder ball sizes. Since the proposed combination references fails to teach or suggest all of the claimed features, Applicant respectfully submits that Claim 11 is patentable over those references at least by virtue of its dependency on Claim 8.

Claims 13 and 18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Lau (U.S. Patent No. 6,075,710). Claims 13 and 18 depend from Claims 8 and 16. As argued above, Nakamura fails to teach or suggest all of the features of Claims 8 and 16. Lau does not cure this deficiency of Nakamura as Lau was cited by the Examiner for its teachings of various chip thicknesses. Since the proposed combination references fails to teach or suggest all of the claimed features, Applicant respectfully submits that Claims 13 and 18 are patentable over those references at least by virtue of their dependency on Claims 8 and 16.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1 and 3-22. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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